WHAT IS CLAIMED IS:

1. An information processing unit, comprising:

a prefetch buffer for fetching an instruction through a bus with its width being twice or more as large as an instruction length, to store the prefetched instruction;

a decoder for decoding the instruction stored in said prefetch buffer;

an arithmetic unit for executing the decoded instruction;

an instruction request control circuit performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded, otherwise performing the prefetch request sequentially to prefetch the instructions; and

a prefetch control circuit fetching the branch target instruction to said prefetch buffer when the branch is ensured to occur by executing the branch instruction, while ignoring the branch target instruction when a branch does not occur.

2. The information processing unit according to claim 1, wherein said prefetch buffer prefetches the instruction from a main memory through an instruction cache memory.

3. The information processing unit according to claim 2, wherein said prefetch control circuit outputs to the instruction cache memory a control signal for canceling the prefetch request, which has

been performed to prefetch the branch target instruction, when the branch does not occur, to thereby prevent an access to the main memory, the access being caused by a cache miss.

4. The information processing unit according to claim 2, wherein said prefetch buffer prefetches the instruction from the instruction cache memory through a bus with its width being twice as large as an instruction length, and outputs the instruction to said decoder through a bus with its width equal to the instruction length.

5. The information processing unit according to claim 4, wherein said prefetch buffer stores four pieces of instructions at maximum.

6. The information processing unit according to claim 1, wherein said decoder and said arithmetic unit perform operations in units of one instruction.

7. The information processing unit according to claim 1, wherein said instruction request control circuit and said prefetch control circuit perform operations to allow, when a delayed branch instruction appears, a branch to occur following an instruction subsequent to the delayed branch instruction.

8. The information processing unit according to claim 1, wherein the branch instruction includes a conditional branch instruction and/or an unconditional branch instruction.

9. The information processing unit according to claim 1, further comprising a register for writing therein an execution result of said arithmetic unit.

10. An information processing method, comprising:

a first prefetch step of prefetching an instruction through a bus with its width being twice or more as large as an instruction length, to store the prefetched instruction;

a decode step of decoding the prefetched instruction;

an execution step of executing the decoded instruction;

an instruction request step of performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded, otherwise performing the prefetch request sequentially to prefetch the instructions; and

a second prefetch step of prefetching the branch target instruction when the branch is ensured to occur by executing the branch instruction, while ignoring the branch target instruction when a branch does not occur.

11. The information processing method according to claim 10, wherein said first prefetch step prefetches the instruction from the main memory from the instruction cache memory.

12. The information processing method according

to claim 11, wherein said second prefetch step outputs to the instruction cache memory a control signal for canceling the prefetch request, which has been performed to prefetch the branch target instruction, when the branch does not occur, to thereby prevent the access to the main memory, the access being caused by a cache miss.

13. The information processing method according to claim 11, wherein said first prefetch step prefetches the instruction from the instruction cache memory through a bus with its width being twice as large as an instruction length, and outputs the instruction to said decode step through a bus with its width equal to the instruction length.

14. The information processing method according to claim 13, wherein said first prefetch step stores 4 pieces of instructions at maximum.

15. The information processing method according to claim 10, wherein said decode step and said execution step perform operations in units of one instruction.

16. The information processing method according to claim 10, wherein said instruction request step and said second prefetch step perform operations to allow, when a delayed branch instruction appears, a branch to occur following an instruction subsequent to the delayed branch instruction.

17. The information processing method according

to claim 10, wherein said branch instruction includes a conditional branch and/or an unconditional branch.

18. The information processing method according to claim 10, wherein said execution step writes an execution result to a register.